Integrated Circuits and Logic Operations Based on Single-Layer MoS_2

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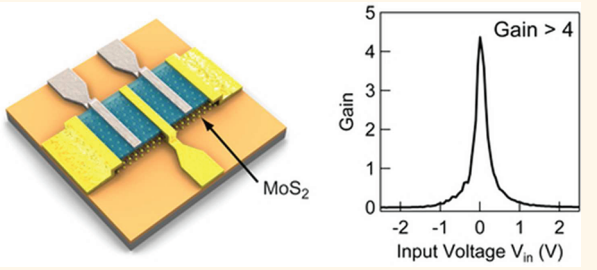
ABSTRACT



Logic circuits and the ability to amplify electrical signals form the functional backbone of electronics along with the possibility to integrate multiple elements on the same chip. The miniaturization of electronic circuits is expected to reach fundamental limits in the near future. Two-dimensional materials such as single-layer MoS_2 represent the ultimate limit of miniaturization in the vertical dimension, are interesting as building blocks of low-power nanoelectronic devices, and are suitable for integration due to their planar geometry. Because they are less than 1 nm thin, 2D materials in transistors could also lead to reduced short channel effects and result in fabrication of smaller and more power-efficient transistors. Here, we report on the first integrated circuit based on a two-dimensional semiconductor MoS_2. Our integrated circuits are capable of operating as inverters, converting logical "1" into logical "0", with room-temperature voltage gain higher than 1, making them suitable for incorporation into digital circuits. We also show that electrical circuits composed of single-layer MoS_2 transistors are capable of performing the NOR logic operation, the basis from which all logical operations and full digital functionality can be deduced.

KEYWORDS: two-dimensional materials · dichalcogenides · MoS_2 · nanoelectronic devices · logic circuits · digital electronics

Two-dimensional materials[1] are extremely interesting as building blocks of next-generation nanoelectronic devices for simple geometric reasons. It is in principle much easier to fabricate circuits and other complex structures by tailoring 2D layers into desired forms than to deposit or grow nanowires or nanotubes with predictable electrical properties in predefined positions. Because of their atomic scale thickness, two-dimensional materials also offer a higher degree of electrostatic control than bulk materials,[2] making them interesting for fabrication of low-power electronic devices.[3] Without any doubt, the most widely studied two-dimensional material to date is graphene,[4] due to its high intrinsic low-temperature mobility of at least 200 000 $cm^2/(V\,s)$,[5] the presence of massless Dirac fermions,[6] and a wealth of interesting physical phenomena such as the fractional quantum Hall effect.[7] In its untreated form however, graphene has no band gap, resulting in small current on/off ratios in graphene field effect transistors. Graphene band gaps up to 400 meV have been introduced by shaping them into ribbons[8,9] or applying high transverse electric fields to bilayer graphene.[10,11] This not only increases complexity but also results in significant mobility reduction or loss of coherence[12] or requires voltages exceeding 100 V.[10] Because of this, it is very difficult to build logic circuits based on graphene that would operate at room temperature with low stand-by power dissipation.

Logic circuits and the ability to amplify electrical signals form the functional backbone of electronics along with the possibility to integrate multiple elements on the same chip. Here, we demonstrate that single-layer MoS_2, a two-dimensional semiconductor with a direct band gap of 1.8 eV (ref 13), has the capability to amplify signals and perform basic logic operations in simple integrated circuits composed of two MoS_2 transistors.[3] Our integrated circuit is composed of two n-type transistors realized on the same two-dimensional crystal of monolayer MoS_2, as schematically depicted in Figure 1a and b.

Single-layer MoS_2 is a typical two-dimensional semiconductor from the layered transition metal dichalcogenide family. Single layers, 6.5 Å thick, can be extracted from bulk crystals using the micromechanical cleavage technique commonly associated with the production of graphene,[1,14] lithium-based intercalation,[15,16] or liquid phase exfoliation[17] and used as ready-made blocks for electronics.[3] Decreasing the number of

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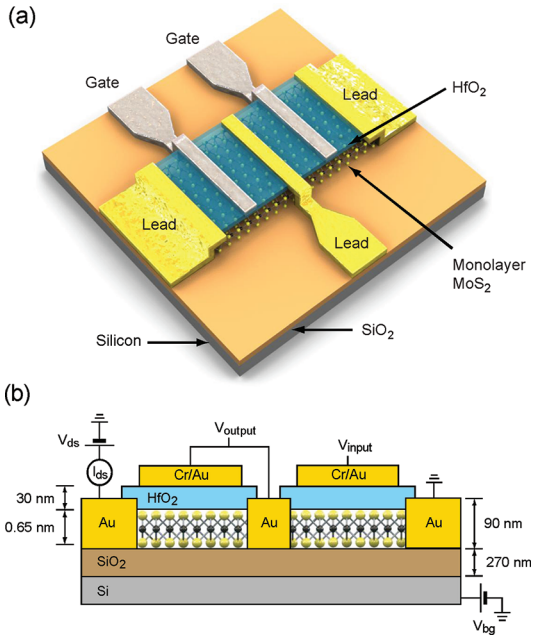

Figure 1. Integrated circuit based on single-layer MoS_2 (not to scale). (a) Single-layer MoS_2 is deposited on top of a Si chip covered with 270 nm thick SiO_2. The integrated circuit is composed of two transistors defined by a neighboring pair of leads and controlled by local gates with HfO_2 gate dielectric. (b) Cross-sectional view of the structure of a monolayer MoS_2 integrated circuit together with electrical connections used to characterize the device. One of the gold electrodes acts as drain while the other, source electrode is grounded. The monolayer is separated from the top gate by 30 nm of ALD-grown HfO_2. The top gate width for the device is 4.7 μm, top gate length is 1.3 μm, and lead spacing is 1.6 μm. The substrate can act as a back gate but is kept grounded during the measurement.

layers in mesoscopic MoS_2 structures leads to a transformation from an indirect band gap semiconductor with a band gap of 1.2 eV (ref 18) into a direct gap semiconductor,[13,19–21] with a band gap of 1.8 eV (ref 13) due to quantum confinement.[21] Being an ultrathin direct gap semiconductor, single-layer MoS_2 is very interesting as a material complementary to graphene that does not have a band gap in its pristine form. This makes it very difficult to fabricate logic circuits[22,23] or amplifiers[24] that would operate at room temperature with a voltage gain > 1, which is necessary for incorporating such structures in electronic circuits. The presence of a band gap in single-layer MoS_2 on the other hand allows the realization of field-effect transistors with room-temperature on/off ratios that can exceed 10^8 (ref 3), which makes them interesting for building logic devices with low power dissipation. Recent simulations also predict that short channel single-layer MoS_2 devices could have higher on-current density than those based on Si,[25,26] a current on/off ratio higher than 10^{10}, a high degree of immunity to short channel effects[2,27] and abrupt switching.[26] All these properties show that MoS_2 could be an interesting material for future applications in nanoelectronics.

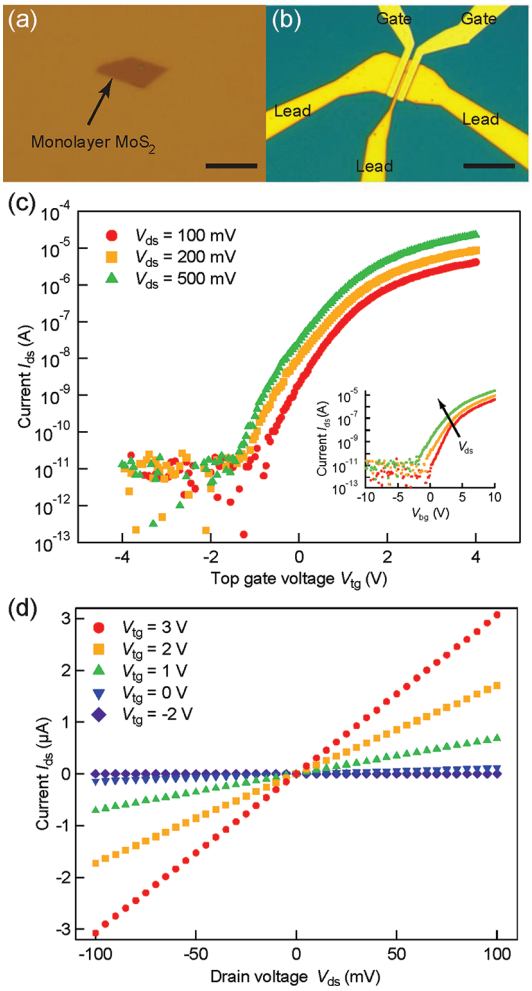

Figure 2. Electrical characterization of the integrated circuit based on monolayer MoS_2. (a) Optical image of a monolayer MoS_2 deposited on top of a Si substrate with a 270 nm thick SiO_2 layer. (b) Integrated circuit based on the flake shown in (a). The device consists of three Au electrical leads that can act as source, drain, and output terminals and two local gates. The scale bars in (a) and (b) are 10 μm long. (c) Drain–source current I_{ds} through the MoS_2 monolayer transistor on the left side of the integrated circuit shown in (b), measured as a function of the top gate voltage V_{tg}. The MoS_2 transistor shows gating response typical of FETs with n-type conducting channels. The inset shows the drain–source current I_{ds} as a function of back gate voltage V_{bg} for drain–source voltage V_{ds} values of 100, 200, and 500 mV. Measurements were performed with floating top gate. (d) Drain–source current I_{ds} as a function of drain–source voltage for different values of V_{tg}. The current through the device changes by over 6 orders of magnitude when the top gate voltage is swept in the −4 to +4 V range.

We begin our integrated circuit fabrication by exfoliating single-layer MoS_2, Figure 2b, from bulk crystals using adhesive-tape-based micromechanical exfoliation,[1,4] commonly used for the production of graphene. Monolayers of MoS_2 are deposited on degenerately doped Si substrates covered with 270 nm thick SiO_2, resulting in optimal contrast for optical detection of single layers.[28] Three electrical leads are first fabricated using standard electron-beam lithography, followed by deposition of 90 nm

thick Au electrodes and annealing in an Ar/H_2 mixture[29] in order to remove resist residue and decrease contact resistance. The device is then covered by atomic layer deposition of 30 nm HfO_2, a high-κ material commonly used as a gate dielectric.[30,31] Finally, local top gates are deposited in the final round of e-beam lithography and metal deposition, resulting in an integrated circuit such as the one shown in Figure 2b, composed of two single-layer transistors connected in series. The channel width of the transistors in our integrated circuit is 4.2 μm, lead spacing is 1.6 μm, and top gate length is 1.3 μm.

Both transistors in our integrated circuit can be independently controlled by applying a voltage V_{tg} to the corresponding top gate, which is one of the crucial requirements for constructing integrated circuits composed of multiple transistors realized on the same substrate. We characterize both transistors in our integrated circuit at room temperature by connecting a pair of neighboring leads to the source and ground terminals of a semiconductor parameter analyzer and a voltage V_{tg} to the corresponding top gate. The substrate is grounded throughout the measurements. The transfer characteristic for the transistor on the right side of the integrated circuit is shown in Figure 2c and is typical of n-type field-effect transistors. By changing the top gate voltage V_{tg} from -4 V to $+4$ V, we can modify the current through the device over several orders of magnitude thanks to the high current on/off ratio of our transistor, higher than 10^6 in this range of top gate voltage V_{tg}. The on-resistance is 24 kΩ for $V_{ds} = 100$ mV and $V_{tg} = 4$ V. The linear and symmetric I_{ds} *vs* V_{ds} characteristics shown in Figure 2d indicate that the contacts are ohmic. From back-gating characteristics, shown in the inset of Figure 2c, we estimate the two-contact low-field field-effect mobility of $\sim$320 cm^2/(V s). At the bias voltage $V_{ds} = 500$ mV, the maximal measured on-current is 22 μA (4.6 μA/μm), with I_{on}/I_{off} higher than 10^6 for the $\pm$4 V range of V_{tg} and an $I_{off} \approx 400$ fA/μm.

The device transconductance defined as $g_m = dI_{ds}/dV_{tg}$ is 12 μS (2.6 μS/μm) for $V_{ds} = 500$ mV and is comparable to CdS nanoribbon array transistors (2.5 μS/μm at $V_{ds} = 1$ V).[32] High-performance top-gated graphene transistors can have normalized transconductance values[33] as high as 1.27 mS/μm, while carbon nanotubes can reach transconductance of 2.3 mS/μm.[34] We expect that lowering the channel length will reduce the number of scattering centers and increase the on-current in MoS_2-based transistors. Theoretical models predict that MoS_2 transistors with a gate length of 15 nm would operate in the ballistic regime[25,26] with a maximum on-current as high as 1.6 mA/μm and a transconductance of 4 mS/μm, for both $V_{tg} = 0.6$ V and a bias $V_{ds} = 0.5$ V.[26]

The efficient channel switching for small voltages exhibited by our device is also clearly illustrated in Figure 2d, where we show the source–drain current

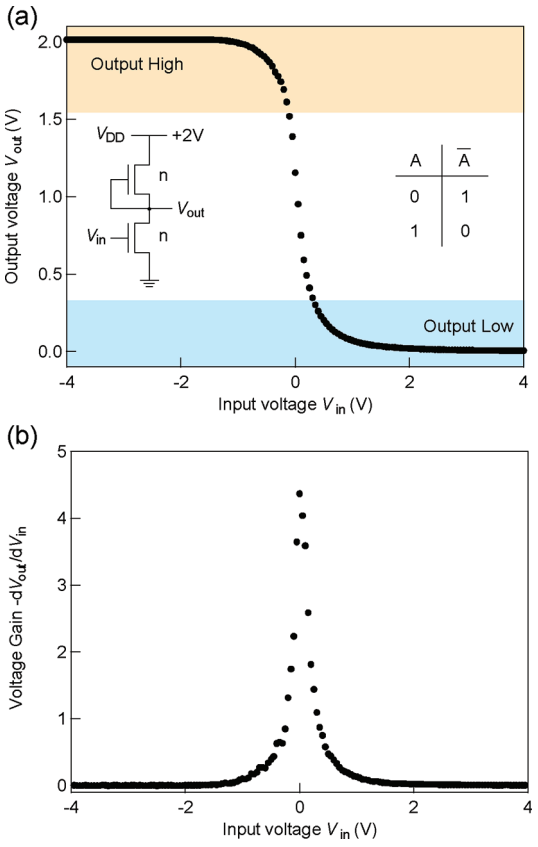

Figure 3. Characteristics of the integrated MoS_2 inverter. (a) Output voltage as a function of the input voltage. Schematic drawing of the electronic circuit and the truth table for the NOT logic operation (inset). (b) Dependence of the inverter gain (negative value of dV_{out}/dV_{in}) on the input voltage. The maximal voltage gain above 4 indicates that our inverter is suitable for integration in arrays of logic devices.

I_{ds} dependence on source–drain voltage V_{ds} for different values of top gate voltage V_{tg}. This large degree of control at room temperature is necessary for realizing logic operations with large voltage gain. For development of logic circuits based on new materials, a voltage gain > 1 is necessary so that the output of one logic gate could be used to drive the input of the next gate without the need for signal restoration.

We proceed by demonstrating that our single-layer MoS_2 integrated circuit can operate as the most basic logic gate: a logic inverter, capable of converting a logical 0 (low input voltage) into logical 1 (high output voltage). We connect the middle lead to one of the local gates in a configuration depicted in the inset of Figure 3a, commonly used in logic circuits based on only one type (n or p) of transistor. In this configuration, the "lower" transistor acts as a switch, while the "upper" one acts as an active load. Input voltage V_{in} is applied to the local gate of the switch transistor while the supply voltage $V_{dd} = 2$ V is applied to the drain electrode of the load transistor. The output voltage and transfer characteristic of the inverter as a function of the input voltage V_{in} is shown in Figure 3a.

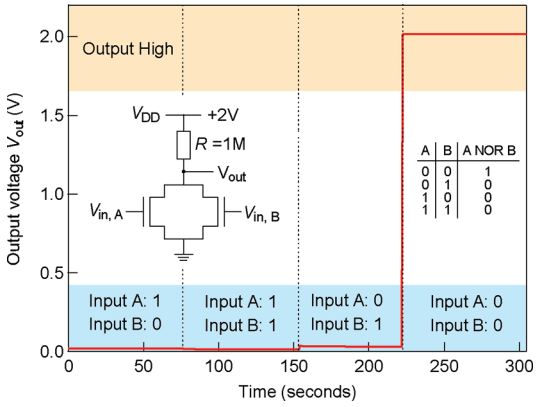

Figure 4. Demonstration of a NOR-gate logic circuit based on single-layer MoS_2 transistors. The circuit is formed by connecting two monolayer MoS_2 transistors in parallel and using an external 1 MOhm resistor as a load (left inset). The output voltage V_{out} is shown for four different combinations of input states (1,0), (1,1), (0,1), and (0,0). The output is in the high state only if both inputs are in the low state (truth table in the inset). All logic operations can be expressed as combinations of NOR operations.

For input voltages corresponding to logic 0, the switch transistor has a higher resistance than the load transistor and is effectively turned off. This results in a constant voltage at the output terminal, which is close to the supply voltage of V_{dd} = 2 V applied to the load drain electrode. By increasing the input voltage above −1 V, the lower FET becomes more conductive and the output voltage V_{out} is now in the low range.

In the input voltage range of ±0.3 V, the output of the inverter is changing faster than the input, indicating that our device is capable of amplifying signals. The voltage gain defined as the negative of dV_{out}/dV_{in} and plotted in Figure 3b is higher than 4. For successful implementation of digital logic in electronic circuits based on any new nanomaterial, a voltage gain > 1 is needed so that the output of one inverter could drive the input of the next inverter in the cascade. Our inverter has a voltage gain higher than 4 and is therefore suitable for integration in arrays of logic gates. This could involve level shifters because the input and output logic levels are not the same. Increasing the threshold voltage of MoS_2 transistors using for example substrate functionalization could also bring input and output voltages to the same level.

We note that to the best of our knowledge the maximal voltage gain for graphene-based inverters[22] demonstrated so far is 2−7 but at the temperature of 80 K,[23,35] due to the low band gap (<100 meV) in bilayer graphene, which prohibits the use of such devices at room temperature.

Our monolayer MoS_2 transistors can also be used to perform logic operations involving two operands. By connecting two transistors in parallel and using an external resistor as load, we can construct a NOR gate, shown in the inset of Figure 4, where we show the output voltage for all the possible input states of the NOR gate. When either one or both of the transistors are in the "on" state (corresponding to V_{in} = 2 V), the output is ~0 V, corresponding to logical 0. Only when both transistors are in the "off" state does the output become logical 1 ($V_{out} \approx V_{dd}$ = 2 V). NOR operation forms a functionally complete set of binary operations: every possible logic operation (AND, OR, NAND, *etc.*) can be realized using a network of NOR gates.

CONCLUSIONS

We have demonstrated here that single-layer MoS_2, a new two-dimensional semiconductor, can be used as the material basis for fabrication of integrated circuits and for performing logic operations with room-temperature characteristics suitable for integration. Our work represents the critical first step in the implementation of digital logic in two-dimensional materials at room temperature. Together with the possibility of large-scale liquid-based processing of MoS_2 and related 2D materials,[17] our finding could open the way to using MoS_2 for applications in flexible electronics. Single-layer MoS_2 also has advantages over conventional silicon: it is thinner than state-of-the-art silicon films that are 2 nm thick[36] and has a smaller dielectric constant (ε = 7, ref 37) than silicon (ε = 11.9), implying that using single-layer MoS_2 could reduce short channel effects[26] and result in smaller and less power-hungry transistors than those based on silicon technology. Several difficulties however need to be solved before MoS_2 can become a mainstream electronic material for the semiconductor industry. A method for large-scale growth of continuous monolayers of MoS_2 or a similar 2D semiconductor will be needed to fabricate more complex integrated circuits with a large number of elements.

MATERIALS AND METHODS

Single layers of MoS_2 are exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide) using the adhesive-tape micromechanical cleavage technique method pioneered for the production of graphene. AFM imaging is performed using the Asylum Research Cypher AFM. After Au contact deposition, devices are annealed in 100 sccm of Ar and 10 sccm H_2 flow at 200 °C for 2 h.[29] ALD is performed in a commercially available system (Beneq) using a reaction of H_2O with tetrakis-(ethylmethylamido)hafnium. Electrical characterization is carried out using National Instruments DAQ cards and a home-built shielded probe station with micromanipulated probes.

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